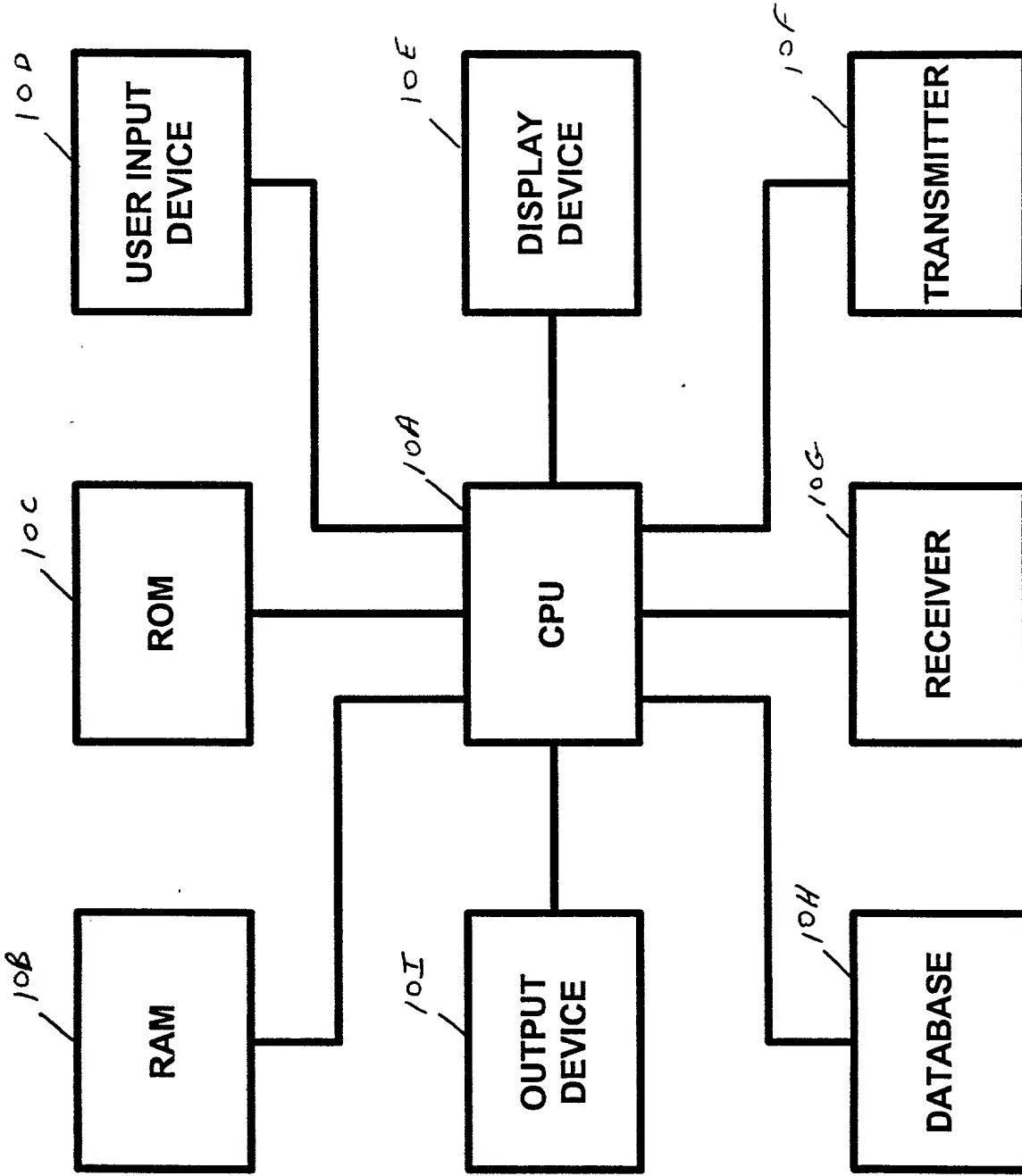


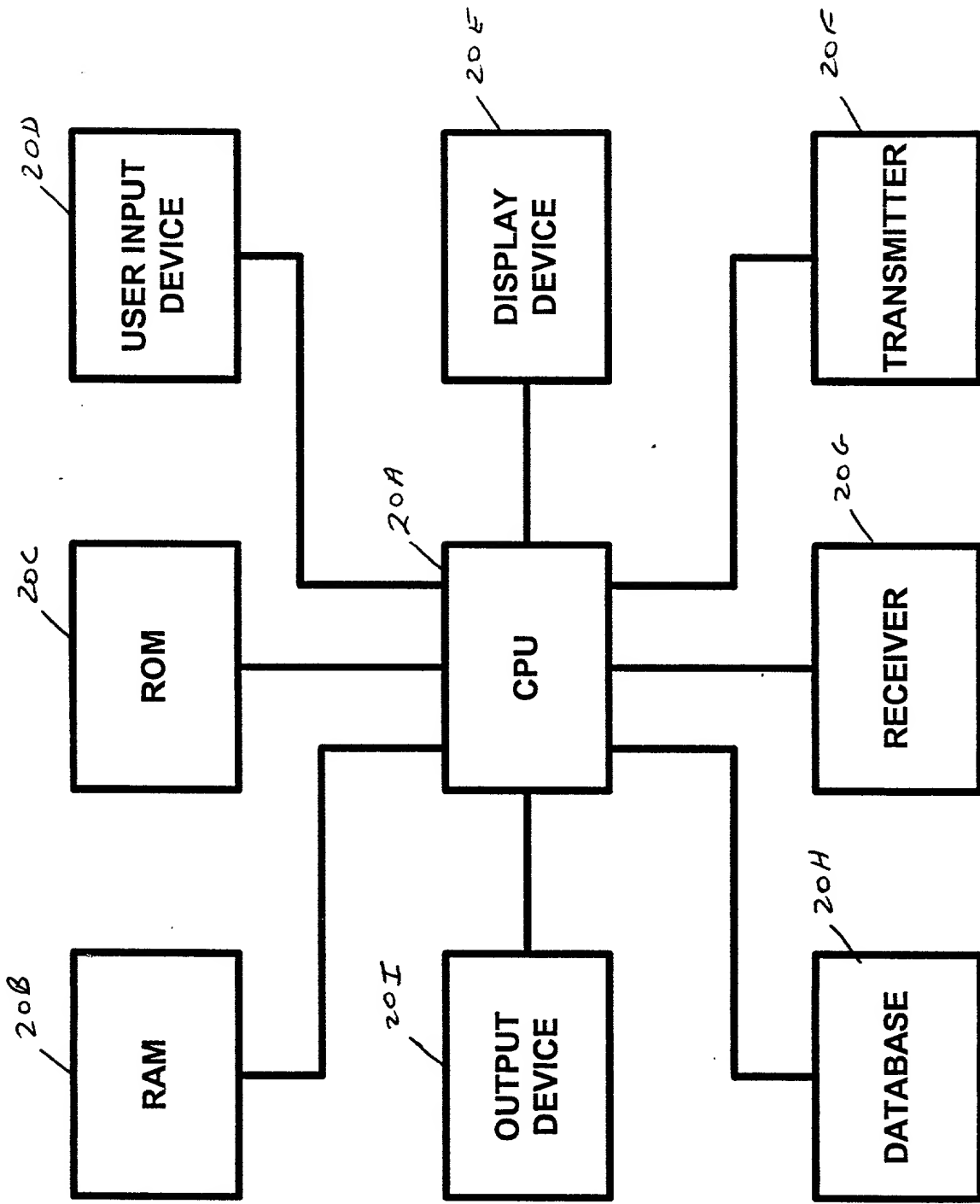
FIG. 1



10-

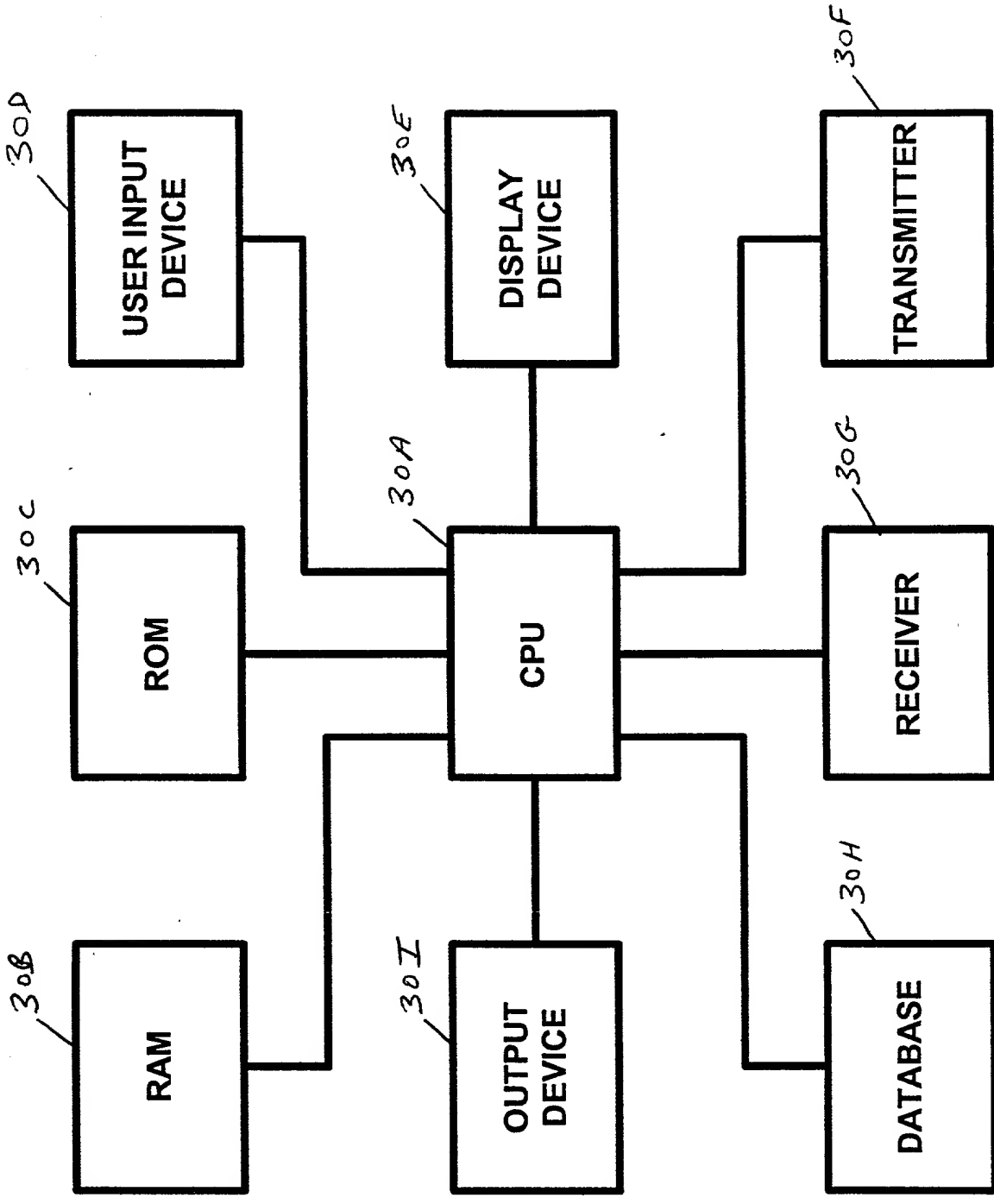
FIG. 2

FIG. 3 is a block diagram of a system 200. The system 200 includes a CPU 20A, a RAM 20B, a ROM 20C, a USER INPUT DEVICE 20D, a DISPLAY DEVICE 20E, a TRANSMITTER 20F, a RECEIVER 20G, an OUTPUT DEVICE 20I, and a DATABASE 20H. The CPU 20A is connected to the RAM 20B, the ROM 20C, the USER INPUT DEVICE 20D, the DISPLAY DEVICE 20E, the TRANSMITTER 20F, the RECEIVER 20G, the OUTPUT DEVICE 20I, and the DATABASE 20H.



20-

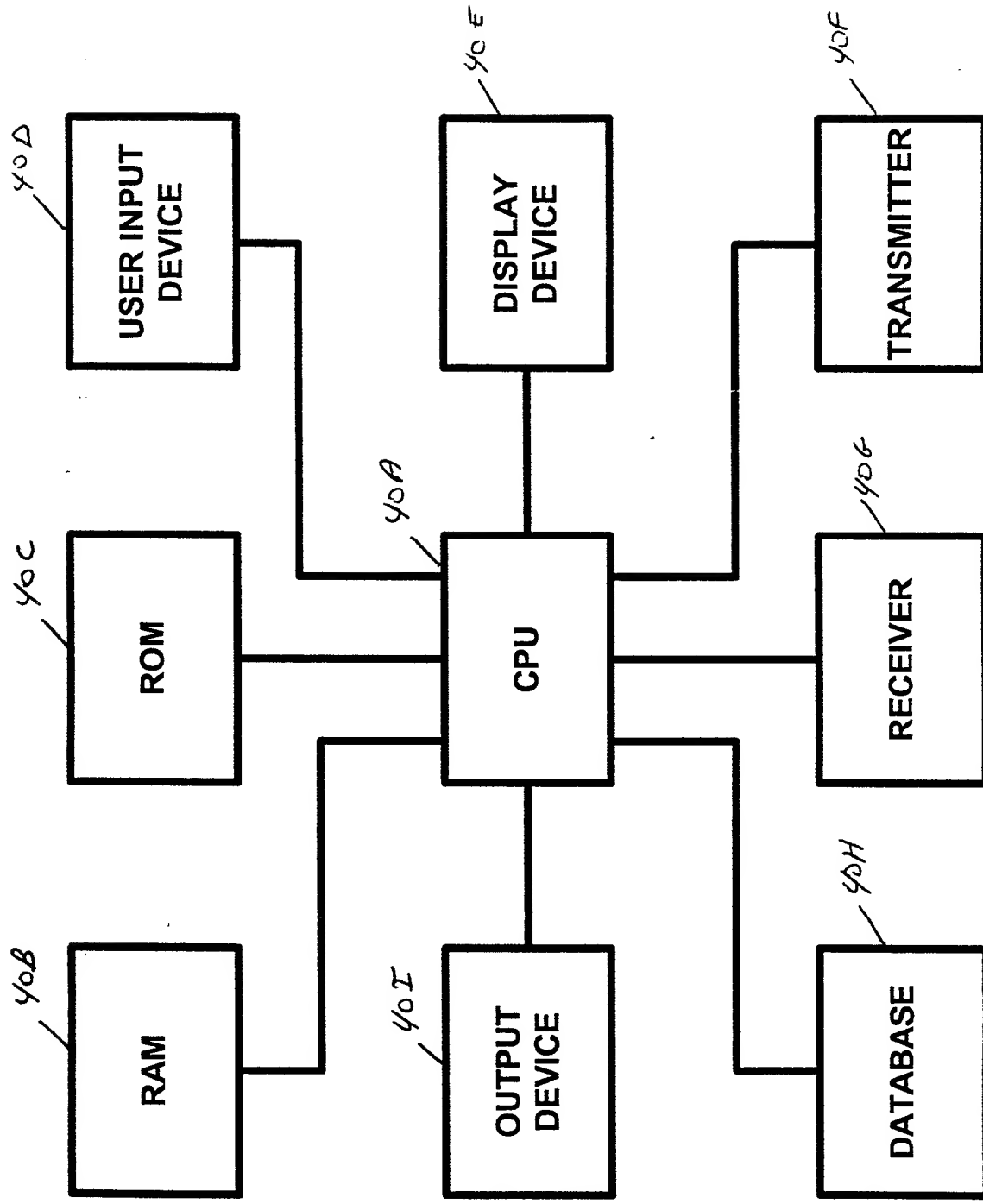
FIG. 3



30-

FIG. 4

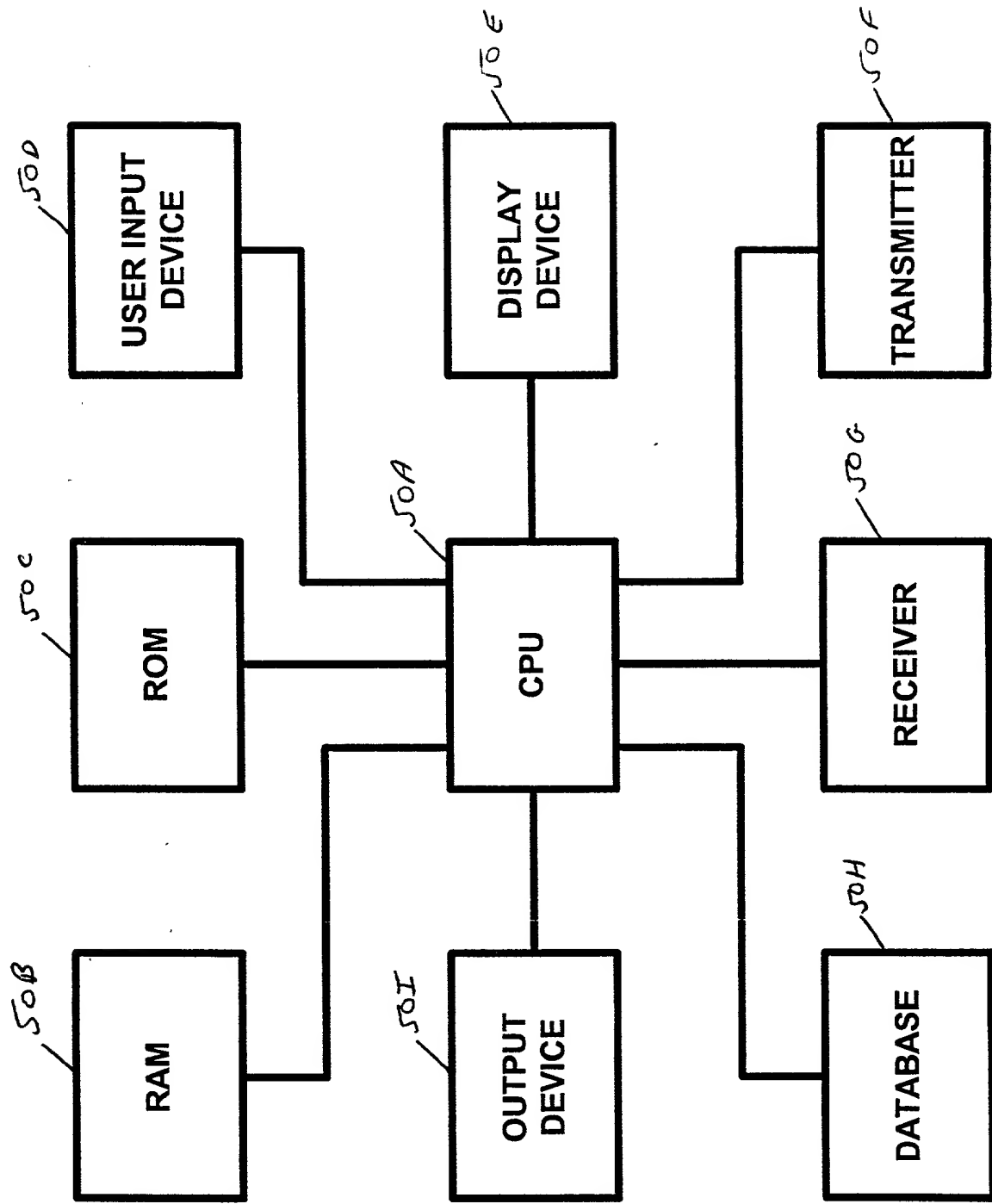
FIG. 5 is a block diagram of a system 400 according to one embodiment of the present invention.



40-

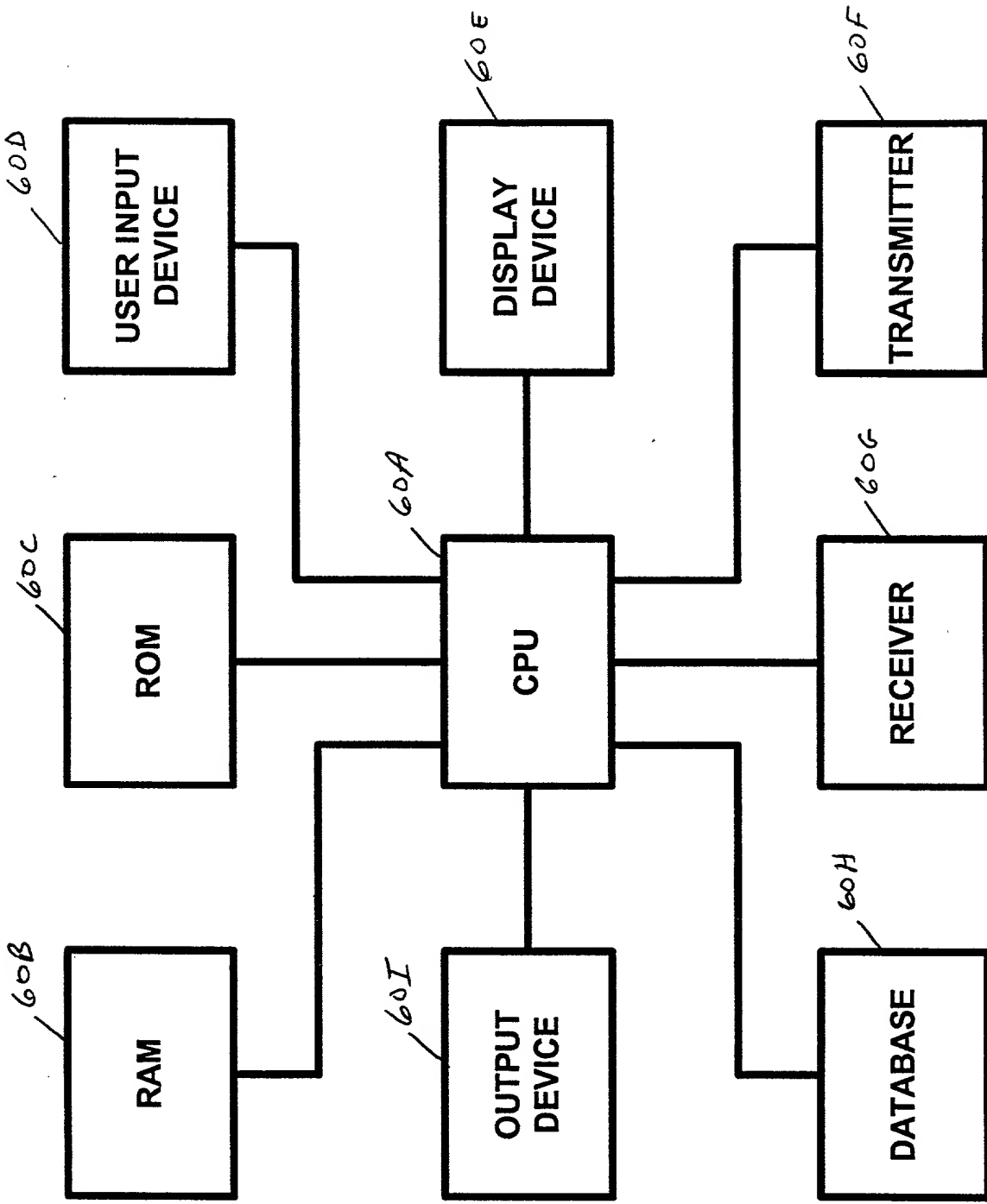
FIG. 5

FIG. 6 is a block diagram of a system 500.



50-

FIG. 6



600

FIG. 7

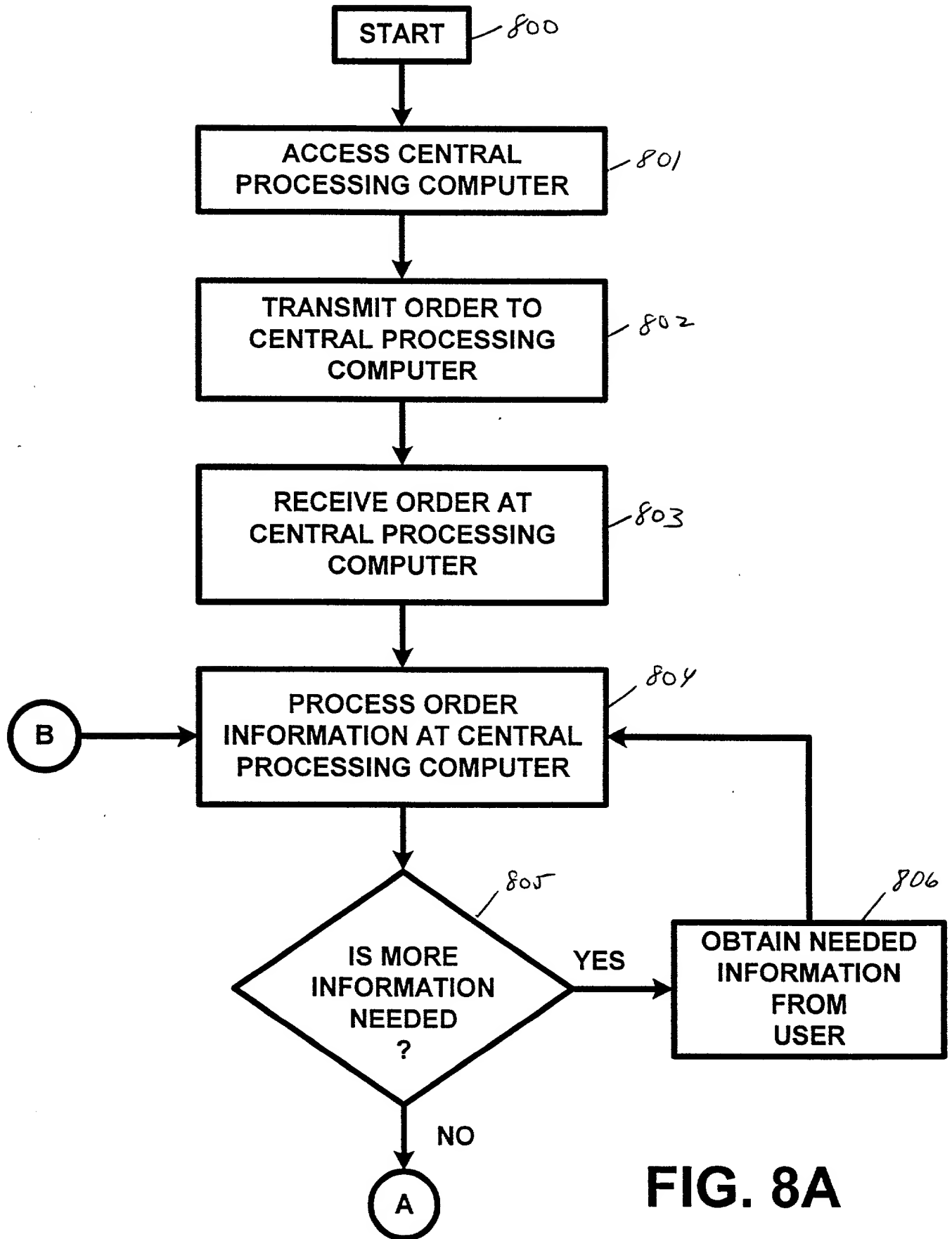


FIG. 8A

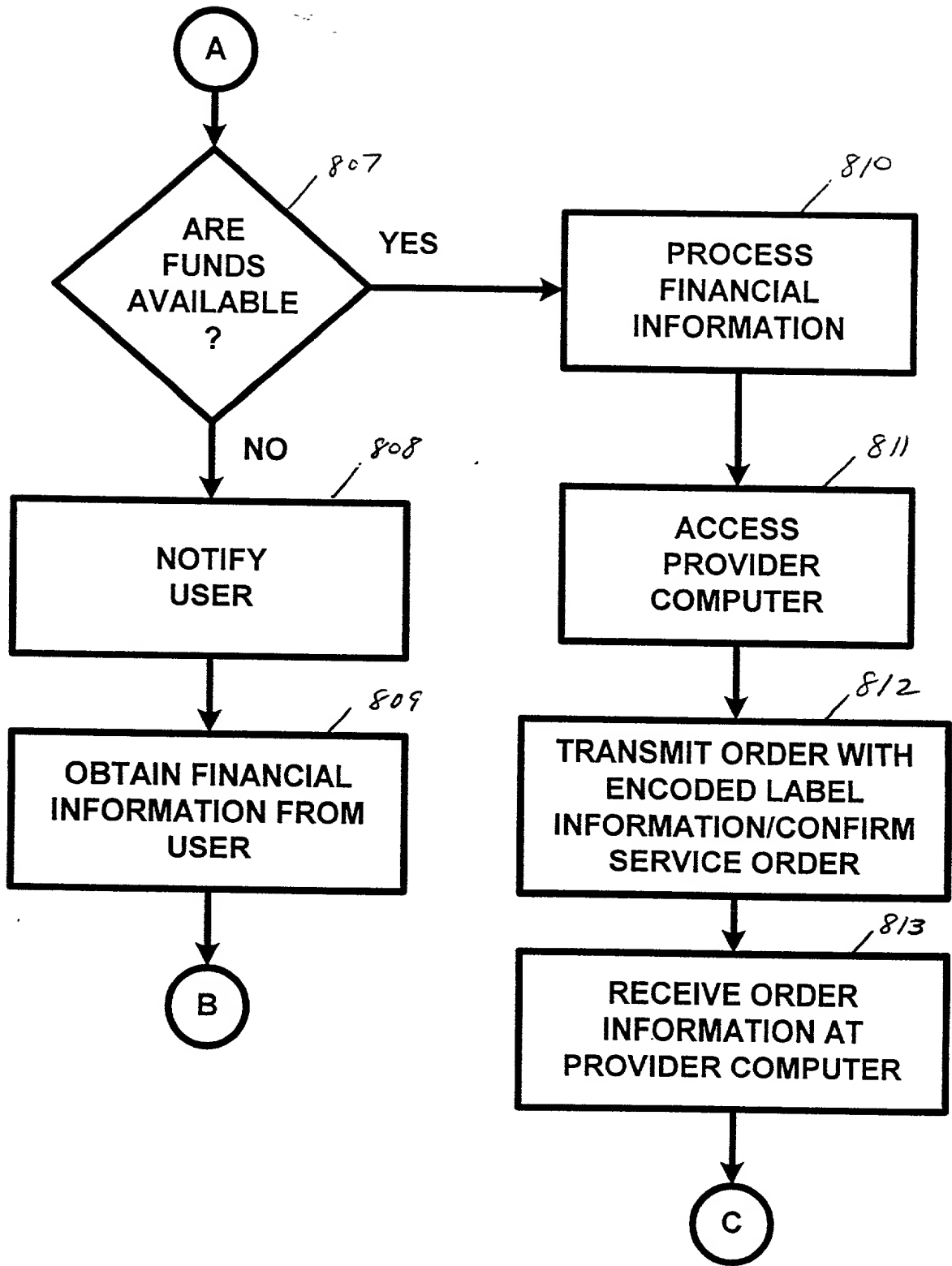


FIG. 8B

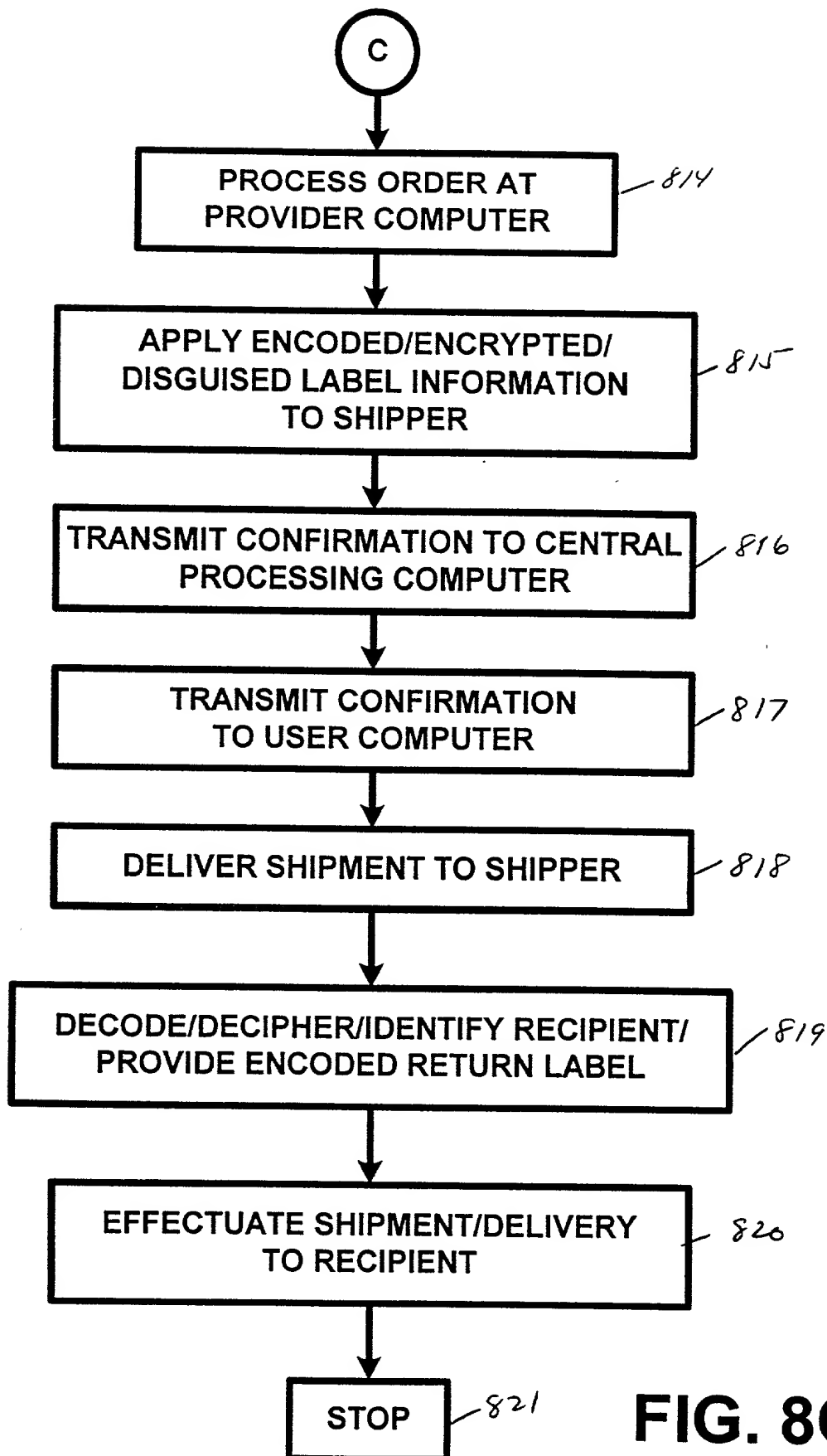


FIG. 8C

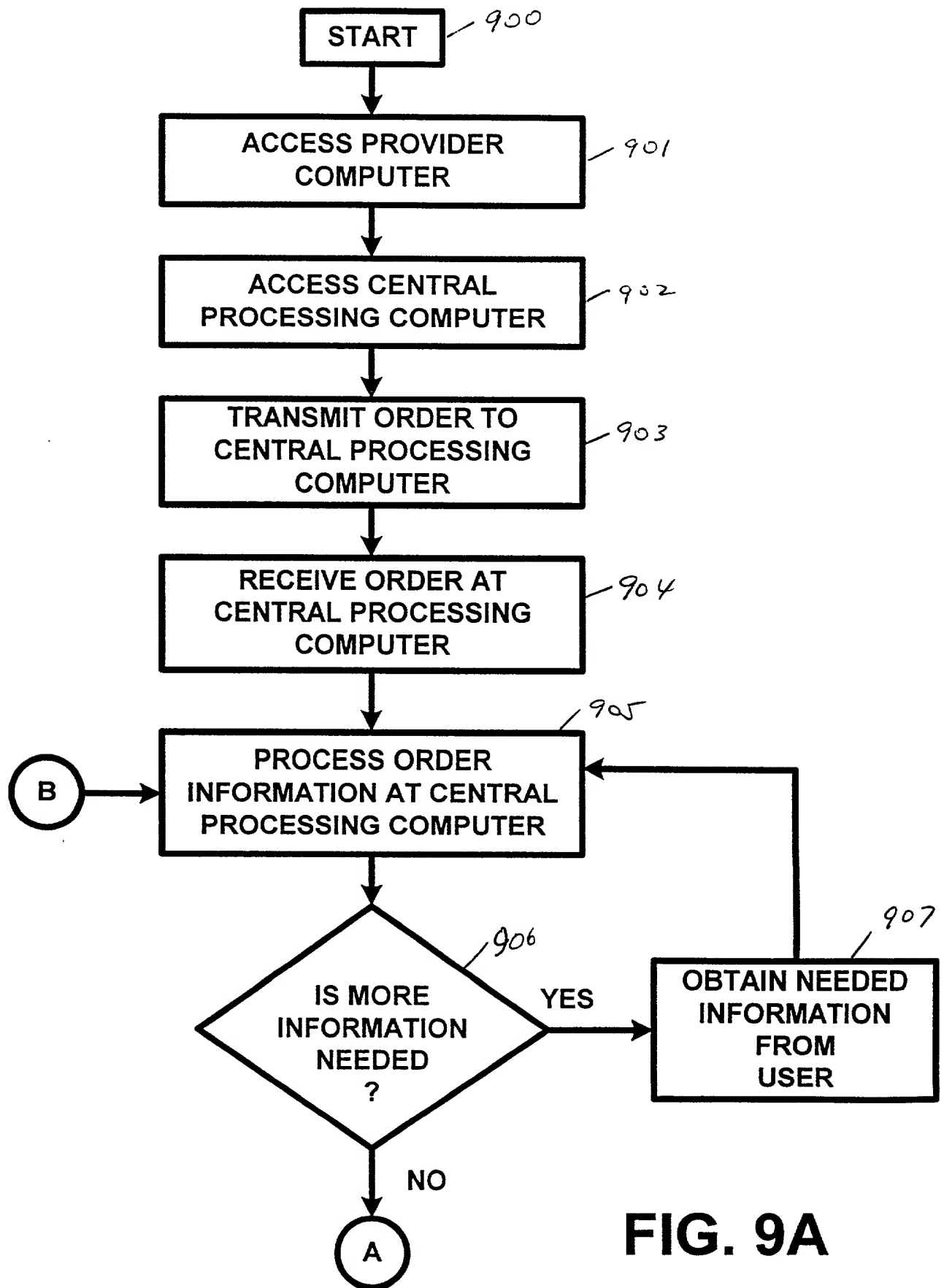


FIG. 9A

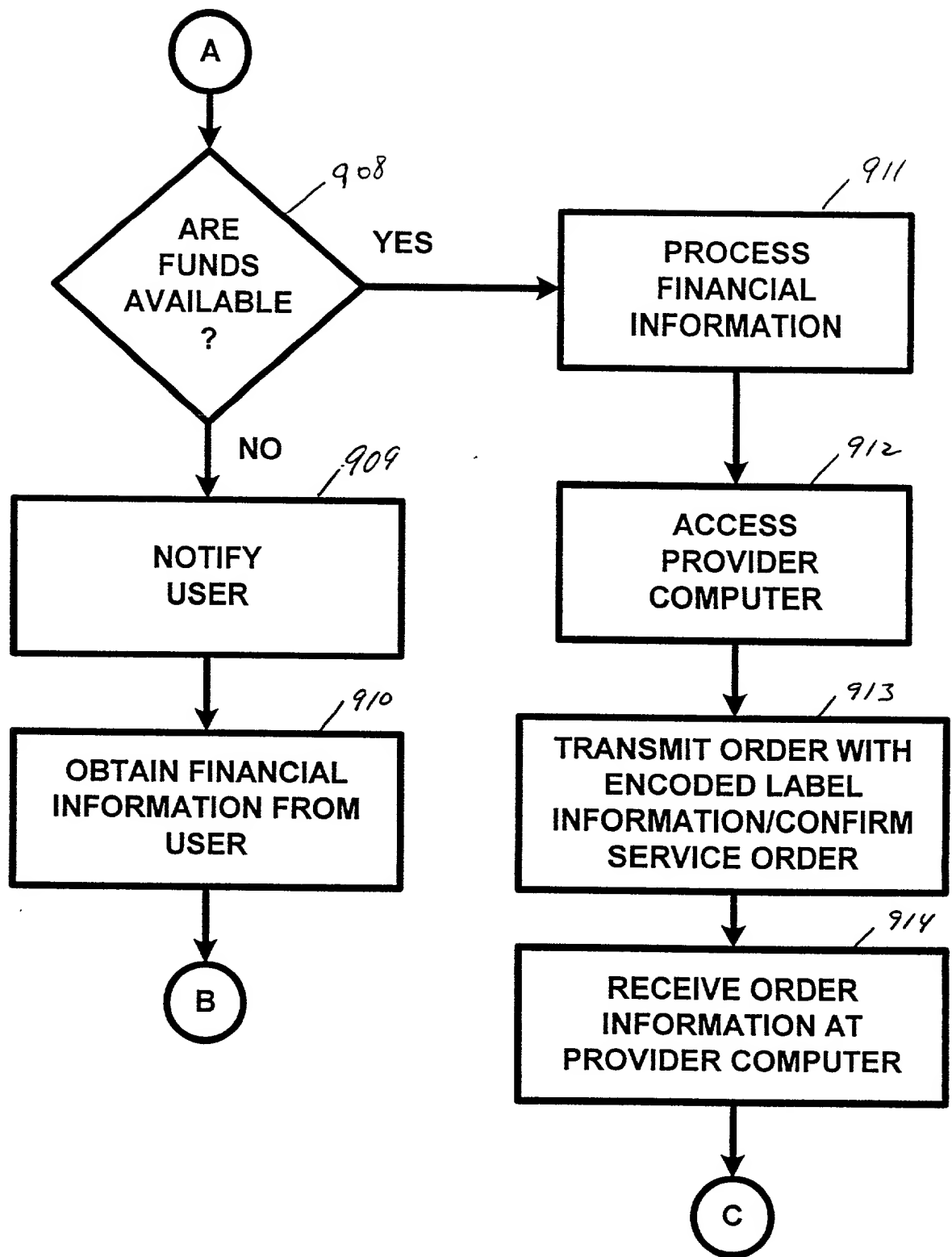


FIG. 9B

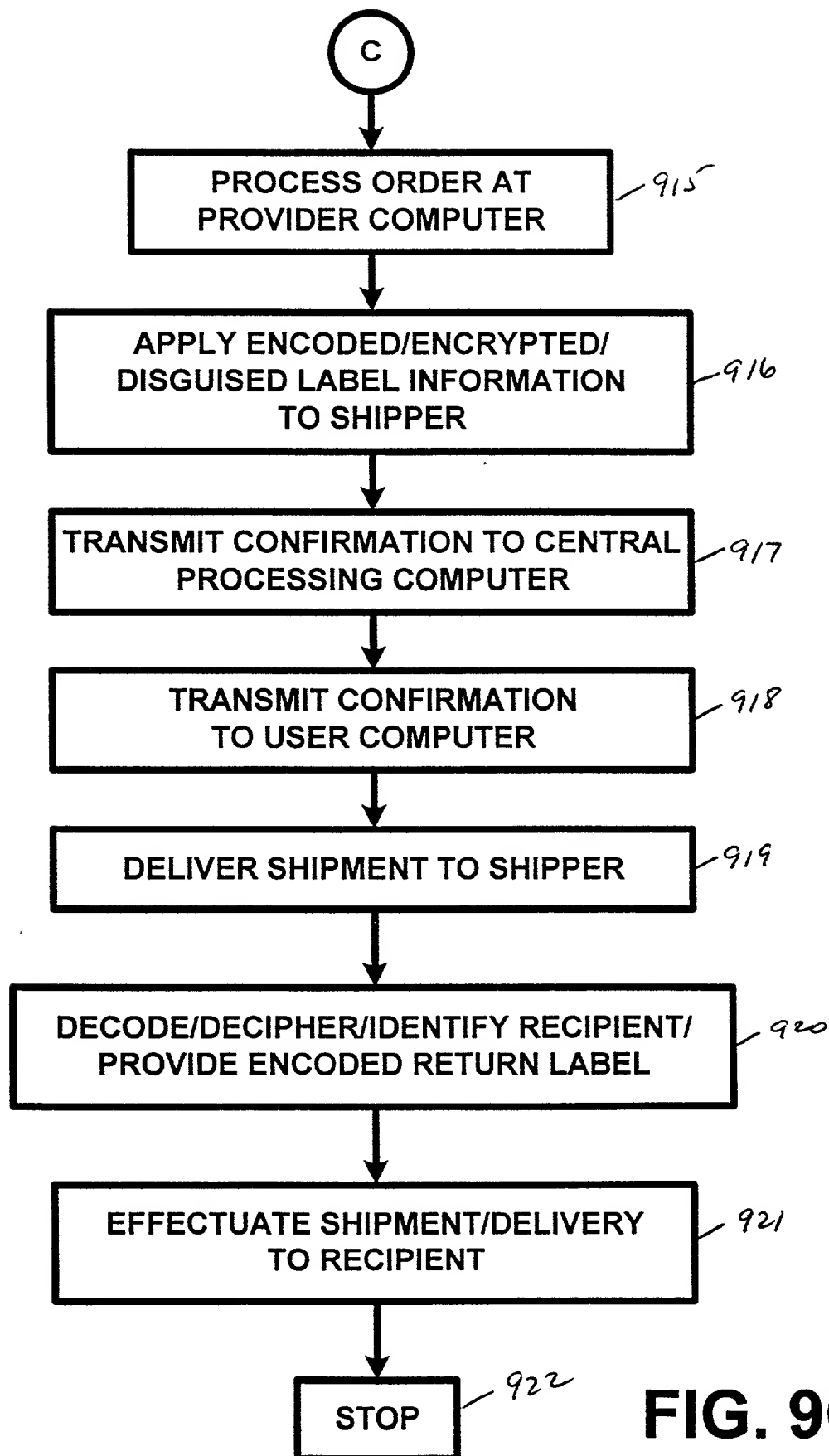


FIG. 9C